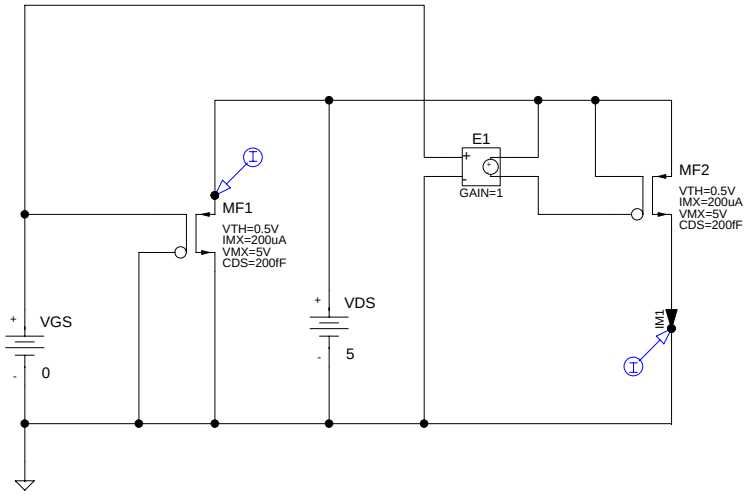


LIBRARY: C:\Projects\Expments\BehavioralComponents\FauxFET.sub

ANALOG INNOVATIONS
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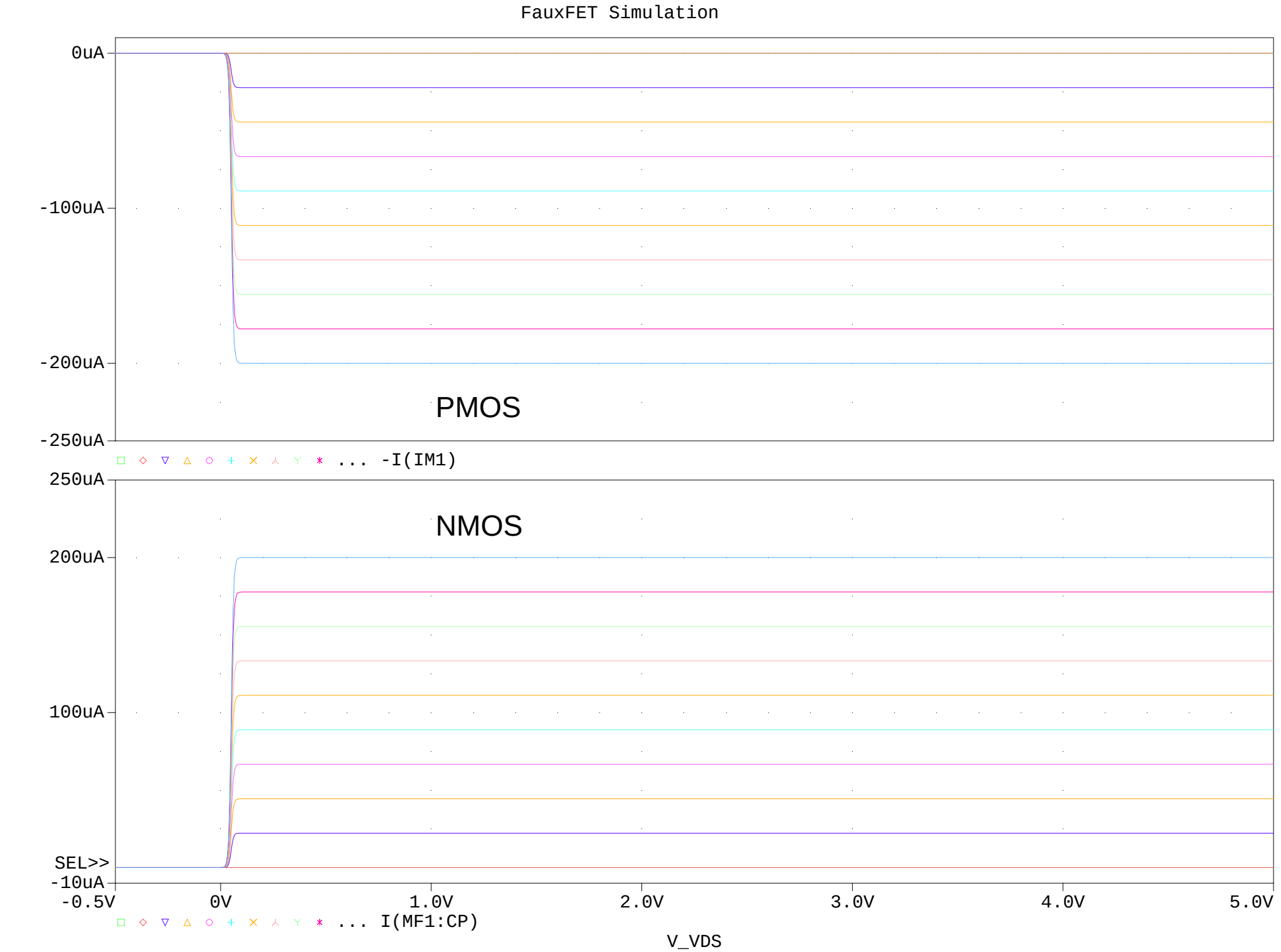
Title:
FauxFET Development

| Size | FileName: | REV |
|---|---|---|
| A | C:\Projects\Expments\BehavioralComponents\FauxFET.sch | A |

February 8, 2014, 8:39 AM


FauxFET Simulation
0uA
-100uA
-200uA
-250uA
PMOS
... -I(IM1)
250uA
NMOS
200uA
100uA
SEL>>
-10uA
-0.5V
0V
1.0V
2.0V
3.0V
4.0V
5.0V
... I(MF1:CP)
V_VDS
Engineer: JT
February 08, 2014

```
********************************************************************************************************************
** FauxFET © 2014 by James E. Thompson, see my page at http://www.analog-innovations.com/
** Behavioral Equivalent to a MOSFET suitable for modeling Logic Blocks
** for Use in Analog Simulators (All Derivatives Exist and are Continuous)
** To emulate an NMOS, connect GN to CN, that node becomes the NMOS Source, CP the NMOS Drain
** To emulate a PMOS, connect GP to CP, that node becomes the PMOS Source, CN the PMOS Drain
.SUBCKT FauxFET CP CN GP GN PARAMS: VTH=0.6V IMX=100uA VMX=5V CDS=200fF
GPN CP CN VALUE {IMX*(V(GP,GN)-VTH)/(VMX-VTH)*(1+TANH(88*(V(GP,GN)-VTH-0.05)))*(1+TANH(88*(V(CP,CN)-0.05)))/4}
CPN CP CN {CDS}
.ENDS FauxFET
********************************************************************************************************************
```